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Electronics Design of the NISS onboard NEXTSat-1

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ABSTRACT

NISS (Near-infrared Imaging Spectrometer for Star formation history) is a unique spaceborne imaging spectrometer (R = 20) onboard the Korea's next micro-satellite NEXTSat-1 to investigate the star formation history of Universe in near infrared wavelength region (0.9 – 3.8 um), with an H1RG IR sensor. NISS electronics system requires to operate the H1RG array as well as to interface to the spacecraft bus system. In this paper, we introduce the requirements and functions of NISS electronics system and the novel readout method to reduce the 1/f noise.

1. INTRODUCTION

NISS (Near-infrared Imaging Spectrometer for Star formation history) is the main payload of NEXTSat-1. NEXTSat-1 is the Korea's third scientific micro-satellite to be launched in 2017. With a total mass less than 136 kg, a size of 60x60x80 cm^3, and 3-axis attitude control in a Sun-synchronous orbit, NEXTSat-1 aims to provide a standard micro-bus to various demands of Korean astronomy and space science communities.

KASI is developing NISS to observe the cosmic NIR background and the emission/absorption spectral lines in the nearby galaxies for investigating the star formation histories from the early universe to local universe (Jeong 2014). In this paper, we introduce the electronics interface requirements and the preliminary design results of NISS electronics in section 2 and in section 3, respectively, while the IR sensor and the readout electronics are discussed in section 4. The summary and the future plan are described in section 5.

2. NISS ELECTRONICS REQUIREMENTS AND SPECIFICATIONS

There are two electronics parts in NISS. The IR sensor and the focal plane electronics are located in a Dewar, which will be cooled down to 80 K by a Stirling cooler. E-box is containing the warm electronics for spacecraft interfaces and instrument controls. Table 1 shows the detail requirements of each electronics board at the design level PDR (Preliminary Design Review). The science data shall be transmitted to the spacecraft via a SERDES interface while we are going to use a CAN bus for the commands and telemetry interfaces. The total power of NISS is estimated about 18 W and the data will be generated as much as 3.9 Gbits per day.

Table 1. NISS Electronics Functional Requirements

Location	Board	Functional Requirements
Dewar	Focal Plane Board (FPB)	- IR sensor harnessing
E-box	AMP	- Bias voltage setting - Analog signal processing/amplifying - A/D conversion
	DSP	- Array clock generating - CAN bus interface to S/C - SERDES interface to S/C - Command processing - HK telemetry managing - Shutter control
	PWR	- DC/DC power conversion - Power control & regulation

To meet the spacecraft bus' requirements, there four types of interfaces between bus and NISS electronics system:

- Power interface
  - Primary power (+28V nominal) with return
  - Secondary power (+28V nominal) with return
- Bi-level command interface
  - Primary/Redundant Cooler on/off commands with return
  - CAN A/B selection command with return
- SERDES interface
  - Primary SERDES (Y0, Y1, Y2, CLK) pairs
  - Secondary SERDES (Y0, Y1, Y2, CLK) pairs
- CAN interface
  - CAN A/B interface

Fig. 1 shows the NISS electronics block diagram with interface definition.

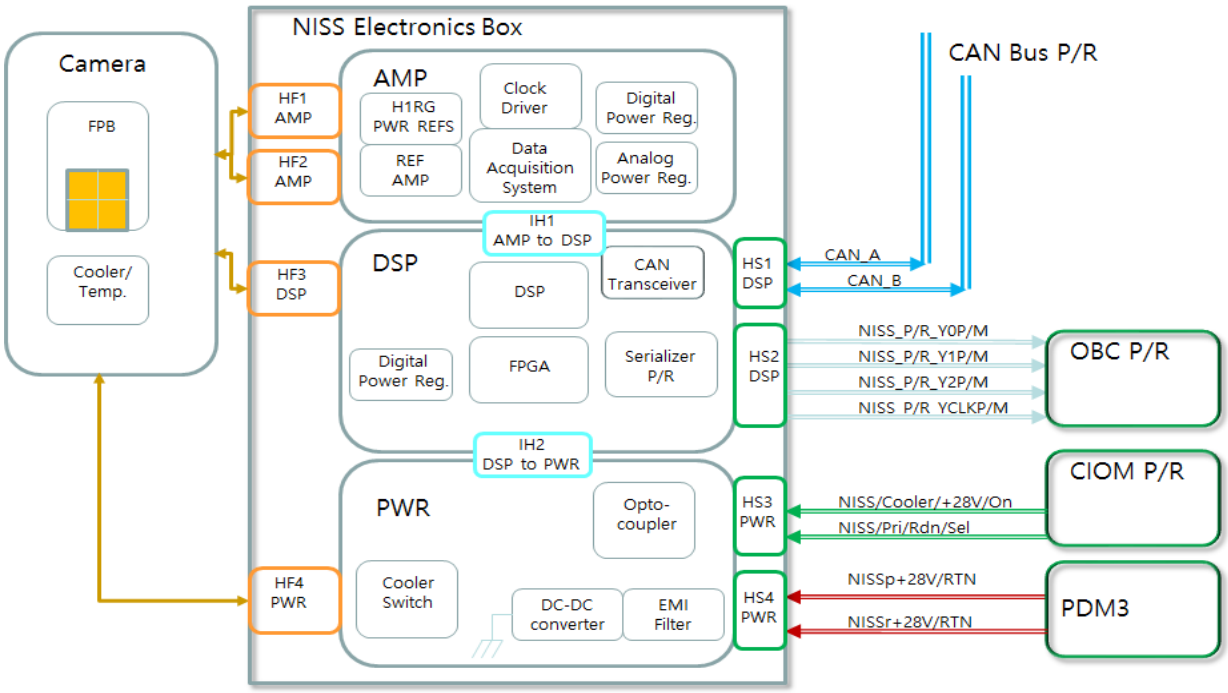

Fig. 1 NISS Electronics Block Diagram

3. NISS ELECTRONICS FUNCTIONAL DESIGN

Based on the functional and interface requirements of NISS electronics, we have designed each electronics board as described.

3.1 Focal Plane Board (FPB)

It has two connectors to interface the H1RG signals to warm electronics. Because the FPB is located in the cooled Dewar (~ 80 K), total 44 lines of Constantan ribbon cables are used for low thermal inputs

3.2 AMP

There are three main functions of AMP board: first is to drive digital clock signals generated from DSP board, second is to provide the clean powers and the reference voltages to the H1RG sensor, and the last is to perform A/D conversions of input analogue signals. We have chosen the Analog Device AD7982 (18bit, 1MSPS, 7mWatt PulSAR) ADC for A/D conversion. It allows four ADC to be daisy chained and read using only 4 wires.

3.3 DSP

To execute various functions of NISS, we use a DSP(TMS320F2812) and a FPGA (ProASIC3E A3PE3000) in the DSP board. The DSP takes control of the CAN interfaces, command processing, and HK telemetry acquisition. The FPGA generates

clock signals for the H1RG array, packetizing received ADC serial data, and operates SERDES interfaces to the bus system. Detailed clock signals for the sensor array is described in the next section.

4. IR SENSOR AND READOUT ELECTRONICS

4.1 IR Sensor

NISS will use a HAWAII-1RG (H1RG) sensor from Teledyne Imaging Sensors. The optimized field of view (2 degree) and pixel scale (15 arcsec) for the NISS science requirements evaluate 480 pixels, therefore 1 K pixels would be enough considering a Nyquist sampling. Although NISS requires specific cut-off frequency (3.8 um) for the array, we have decided to use a standard product (5.3 um) and to insert a blocking filter in front of the sensor for the sake of cost. In this way the dark current would increase about 40 times from ~0.05 e-/pixel/sec (3.8 um @ 80 K) to ~2 e-/pixel/sec (5.3 um @ 80 K) (Beletic et al. 2008), which is tolerable by the sensitivity requirements.

4.2 Readout Electronics

In NISS, we will use 2 outputs with slow mode (100 kHz) to reduce the readout electronics. The descriptions of the digital signals needed to scan the array in Slow Mode described in the technical document are as follow :

- **FSYNCB** : Frame Synchronization Bar (input, active-low). FYSNCB prepares the vertical scanner for the readout of a new frame.
- **VCLK:** Vertical Shift Register Clock (input). It controls the shift register of the vertical (slow) scanner. Every falling edge of VCLK advances the pattern in the shift register by one cell (row).
- **LSYNCB:** Line Synchronization Bar (input, active-low). LSYNCB prepares the horizontal scanner for the readout of a new line.
- **HCLK:** Horizontal Shift Register Clock (input). It controls the shift register of the horizontal (fast) scanner. Every falling edge of HCLK (or every edge, if the on-chip clock divider is disabled) advances the pattern in the shift register by one cell (column).
- **READEN:** Read Enable (input). It connects all pixels that belong to the row currently selected by the vertical scanner to the individual vertical read busses. An internal pull-up resistor keeps READEN high if there is no external signal driving the pin.
- **RESETEN:** Reset Enable (input). It performs a reset of all pixels that are currently selected by the vertical and horizontal scanner. It also updates the flip-flops' that store the positions of the columns selected for reset by the horizontal scanner so a whole line can be reset at once.

For removing the large offset voltage at the pixel outputs, two ways are considered: either by using external reference voltage close to the average pixel outputs, or by using the array dedicated reference pixel REFOUT. We tested that the histogram of REFOUT method is slightly tighter than that of external reference voltage

method, we will use the latter because it is easier to implement. The REFOUT will be treated as an individual data channel, much like the rest pixels, to be measured along with other array offsets, such as VRESET, VDSUB, VBIASPOWER and VBIASGATE.
Besides, we will apply a modified Guide mode, or a REFROW removal method, to mitigate 1/f noise. The REFROW removal method is a way to decorrelate the readout 1/f noise by periodically inserting a Reference Pixel Row (REFROW) during the array frame scan. Because the REFROW uses the same ROIC readout as a live pixel row, we will be able to decorrelate the common for them noises due to the readout which have correlation length larger than the length of one row scan in case we insert REFROW each other live pixel row.

5. SUMMARY

NISS is a unique spaceborne imaging spectrometer (R = 20) onboard the Korea's next micro-satellite NEXTSat-1 to investigate the star formation history of Universe in near infrared wavelength region (0.95 – 3.8 um). With an H1RG IR sensor and compact electronics system, we will apply a novel readout method to reduce the 1/f noise for NISS.

REFERENCES

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